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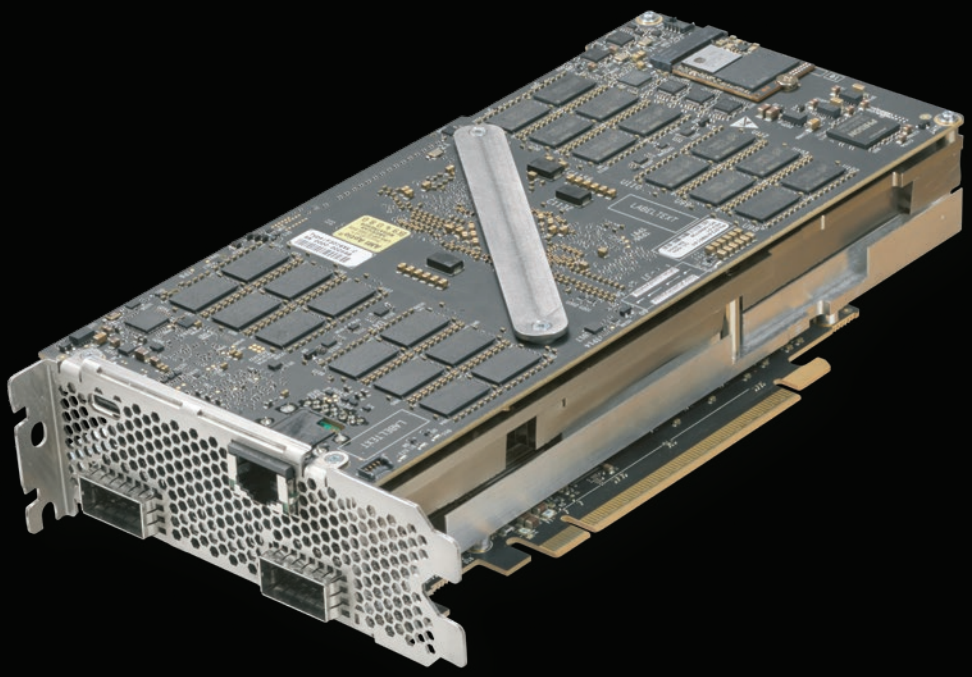
SMARTNIC+DPU SOLUTIONS

Napatech DPU F3076X

DATA SHEET



Powerful Intel®/Altera®-based Data Processing Unit (DPU)
The Napatech DPU F3076X is a 400G PCIe Gen5 card with an Agilex™ AGI041 FPGA and an Intel® Xeon® 6 32-core SoC. The F3076X is based on Intel's DPU architecture, and the unique combination of FPGA and full-fledged Xeon® 6 CPU on a PCI card allows for unique offload capabilities. The Agilex™ AGI041 FPGA provides 2x100/200Gbps Ethernet, 3x PCIe Gen 5.0 interfaces, and plenty of resources to support a 400G pipeline for line rate processing of data. One PCIe Gen 5.0 interface connects to the host, whereas another PCIe Gen 5.0 interface provides full 400G bandwidth between the FPGA and the Xeon® 6 SoC. A third PCIe Gen 5.0 interface could be used for additional 16 lanes of PCIe to the host or provide an expansion port to remote PCIe devices, such as NVMe storage. Compute Express Link (CXL) over the host interface and the expansion port provides high bandwidth and low latency memory and resource sharing, supporting key computing use cases like artificial intelligence (AI) and machine learning (ML). 400G with no bottlenecks!

Customization on demand
The F3076X offers both programmable hardware and software, to tailor the DPU to the most demanding and specific needs in your network, and to modify and enhance its capabilities over the life of the deployment. The Napatech Link-Programmable™ software package for F3076X includes documentation, tools, configurations, and sample code to kick-start development of FPGA bitstreams and Xeon® 6 applications.

Target applications
The DPU F3076X is the perfect solution for network, storage and security offload and acceleration. It enables virtualized cloud, cloud-native or bare-metal server virtualization with tenant isolation.

In the era of exponential data growth, storage is the backbone of enterprise innovation. DPUs are the game-changers that transform your storage services from ordinary to extraordinary. By handling storage management tasks independently from CPUs, DPUs increase data transfer speeds, improve input/output operations per second (IOPS), and provide rapid access to vital information, all while significantly reducing latency.

With DPUs managing encryption, authentication, and access controls at the hardware level, sensitive information is protected without performance trade-offs. By offloading security workloads from overburdened CPUs, DPUs deliver real-time threat detection, seamless encryption, and granular access controls—without sacrificing performance.

DPUs deliver lightning-fast processing and data movement, dramatically reducing bottlenecks and latency in AI pipelines. By intelligently offloading non-computational tasks, DPUs allow CPUs and GPUs to dedicate their cycles entirely to AI training, inference, and analytics.

SOLUTION HIGHLIGHTS

FPGA Device and Memory
- Agilex™ AGIC041
- 4M LEs, 1356.1K ALMs, 17.1K M20Ks
- Crypto support: AES, SM4
- 4x4 GB DDR4-2666MT/s (40b + ECC)

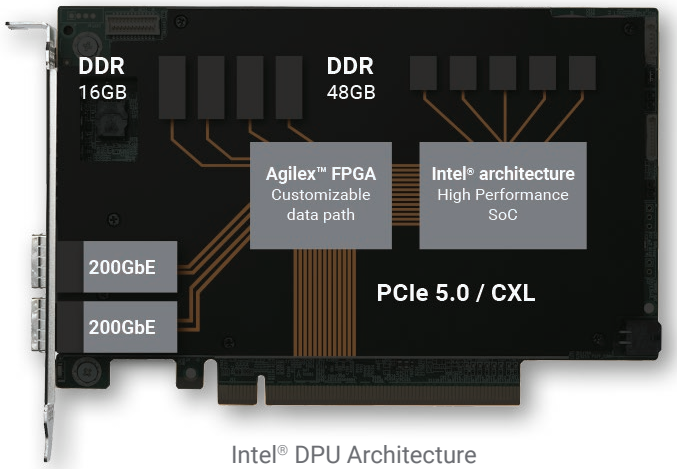
SoC Device and Memory
- Intel® Xeon® 6532P-B Processor
  - 32 cores
  - 128M Cache
  - 2.20 – 3.90 GHz
- 4x12 GB DDR5-5600MT/s (64b + ECC)
- Up to 2 TB in M.2 NVMe x4 (2230) slot for Operating System and applications

PCI Express Interfaces
- 3x PCIe Gen 5.0 x16 (32 GT/s)
  - Card edge host interface, CXL 2.0 (mount option)
  - Expansion port, CXL 2.0 (mount option)
  - Mezzanine interface between FPGA and SoC

High-Speed Network Interfaces
- 2-ports QSFP-DD
- 1x400G, 2x200G, 4x100G, 8x50G, 4x40G, 16x25G, 16x10G

Form Factor, Power and Cooling
- Dual-slot, full-height, 3/4-length
- Passive cooling
- PCI Express ATX AUX power connector
- Max 375W power dissipation supported by platform
- Typical power consumption: (depending on workload)
- Max 5.0W power consumption per QSFP

Board Management
- Integrated BMC
- HW RoT (option)
- Secure boot and configuration
- Secure FPGA image update
- RJ45 1000Base-T management port
- USB-C port connected to SoC
- UART debug interface to SoC
- Wake-on-LAN
- MCTP over SMBus
- Dedicated NC-SI RBT internal port
- PLDM for Monitor and Control (DSP0248)
- PLDM for FRU (DSP0257)



Intel® DPU Architecture

SoC Operating System
- Linux
- UEFI BIOS
- PXE Boot support
- Full shell access via SSH and UART

Operating Environment
- Temperature: -5 to +45 deg. C at >= 4.0 m/s airflow
- Humidity: 5 – 85%
- ASHRAE class A2

Regulatory Approvals and Compliances
- PCI-SIG®, CE, CB, RoHS, REACH, cURus (UL)
- FCC, ICES, VCCI, RCM

Accessories
- FPGA Download Cable (JTAG)
- UART console cable
- Active cooling (blower) mount option

Napatech Software
- Link-Programmable™
- Documentation, HW specification
- Configuration files and FPGA pinout
- Tools and sample code

Target Applications
- Cloud tenant services
- AI Infrastructure
- Disaggregated storage
- Storage services
- Cyber security
- Fintech

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